IN THE CLAIMS

In order to place promptly the application in a condition for allowance, Applicants cancel claims 11-12, 14-22, 26-30, and 32-35 without prejudice. These claims will be presented in a subsequent continuation or continuation-in-part application.

Claim 31 now incorporates the Examiner's comments and is written in independent form. Also, per a previous phone conversation with the Examiner, Claim 13 is now written in independent form as suggested by the Examiner. Thus, it is respectfully submitted that the amended Claims 13 and 31 are now allowable.

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims

We claim:

1. (Original) A data-directed frequency acquisition loop for synching to a signal, the data-directed frequency acquisition loop comprising:

a VCO having an I and Q output;

a first multiplier having as input the signal and the I and Q output, the first multiplier having an I' and Q' output;

a second multiplier having as input the I' and Q' output and having an I'' and Q'' output;

a first low-pass filter having as input the I'' output and having a filtered I'' output;

a third multiplier having as input the filtered I'' output and the Q'' output and having a real output; and

a second low-pass filter having as input the real output and having a feedback output that is input to the VCO.

2. (Original) The data-directed frequency acquisition loop of Claim 1, wherein the second low-pass filter has a gain greater than 1.

3. (Original) The data-directed frequency acquisition loop of Claim 1, further comprising an amplifier, and wherein the feedback output is passed through the amplifier before being input to the VCO.

4. (Original) The data-directed frequency acquisition loop of Claim 1, further comprising a third low-pass filter, and wherein the I' and Q' output are passed through the third low-pass filter before being input to the second multiplier.

5. (Original) The data-directed frequency acquisition loop of Claim 1, wherein the second multiplier is a squarer.

6. (Original) A data-directed frequency acquisition loop for synching to a signal, the data-directed frequency acquisition loop comprising:

a VCO with an I and Q output;

a first multiplier that receives the signal and the I output and generates an I' component from them;

a second multiplier that receives the signal and the Q VCO output and generates a Q' component from them;

a third multiplier that receives the I' and Q' components and generates an I'Q' signal from them;

an amplifier that receives the I'Q' signal and generates a 2I'Q' signal from it;

a fourth multiplier that receives the I' component and generates an I'^2 signal from it;

a fifth multiplier that receives the Q' component and generates a Q'^2 signal from it;

a summer that receives the I'^2 and Q'^2 signals and generates a $I'^2 - Q'^2$ signal;

a first low pass filter that receives the $I'^2 - Q'^2$ signal and generates a filtered $I'^2 - Q'^2$ signal;

a sixth multiplier that receives the 2I'Q' signal and the filtered $I'^2 - Q'^2$ signal and generates a raw VCO driving signal from them;

a second low pass filter that receives the raw VCO driving signal, generates a filtered VCO driving signal from it, and sends the filtered VCO driving signal to the VCO.

7. (Original) The data-directed frequency acquisition loop of Claim 6, wherein the first and second multipliers are limited to multiplying by 1 and –1.

8. (Original) The data-directed frequency acquisition loop of Claim 6, wherein the fourth and fifth multipliers are look-up tables that give the square of the input.

9. (Original) The data-directed frequency acquisition loop of Claim 6, further comprising a second amplifier positioned between the first low pass filter and the sixth multiplier.

10. (Original) The data-directed frequency acquisition loop of Claim 9, wherein the second amplifier is a hard limiter.

11. (Cancelled)

12. (Cancelled)

13. (Currently amended) A frequency acquisition loop that synchronizes with a signal using both a magnitude of error and a direction of error that are generated by convolving data in the signal, the frequency acquisition loop ~~of Claim 11,~~ comprising:

a Costas loop having a VCO;

a sub-circuit that generates $I^2 - Q^2$;

a multiplier that changes the sign of a VCO driving voltage when $I^2 - Q^2$ is less than zero.

14. (Cancelled)

15. (Cancelled)

16. (Cancelled)

17. (Cancelled)

18. (Cancelled)

19. (Cancelled)

20. (Cancelled)

21. (Cancelled)

22. (Cancelled)

23. (Original) A frequency acquisition loop comprising:

a Costas loop having a VCO;

a sub-circuit that generates a difference of a square of an in-phase signal component and a square of a quadrature component;

a multiplier that changes the sign of a VCO driving voltage when the difference is less than zero.

24. (Original) The frequency acquisition loop of claim 23, wherein the multiplier does not change the magnitude of the voltage to the VCO when the difference is less than zero.

25. (Original) The frequency acquisition loop of Claim 23, further comprising a complex multiplier that performs a fully-complex squaring operation.

26. (Cancelled)

27. (Cancelled)

28. (Cancelled)

29. (Cancelled)

30. (Cancelled)

31. (Currently amended) A frequency acquisition and phase-lock loop that provides frequency acquisition and phase lock derived from a signal's data, the frequency acquisition and phase-lock loop ~~of Claim 28,~~ comprising:

a Costas loop having a VCO;

a sub-circuit that generates a difference between an in-phase component squared and a quadrature component squared;

a multiplier that changes the sign of a VCO driving voltage when the difference between an in-phase component squared and a quadrature component squared is less than zero.

32. (Cancelled)

33. (Cancelled)

34. (Cancelled)

35. (Cancelled)

36. (Original) A synch loop for providing frequency acquisition and phase-lock loop for a double sideband suppressed carrier signal, the loop comprising:

a Costas loop having a VCO;

an in-phase loop that generates $I^2 - Q^2$, the in-phase loop including a multiplier that changes the sign of a VCO driving voltage when $I^2 - Q^2$ is less than zero;

wherein the frequency acquisition and phase-lock loop provides frequency acquisition and phase lock derived from the signal's data by generating both magnitude of error and a direction of error that are generated by convolving data in the signal; and

wherein the synch loop has four points of stable equilibrium distributed 90 degrees from one another.